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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,662	01/29/2004	Raied N. Mazahreh	X-1527 US	8551

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XILINX, INC
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EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,662	MAZAHREH ET AL.	
	Examiner	Art Unit	
	Fritz Alphonse	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen (US Pub. No. 20030097633) in view of Van Stralen (U.S. Pat. No. 6,304,996).

As to claims 16 and 30, Nguyen (fig. 4) discloses a turbo decoder system, comprising an input circuit (48) configured to receive a data block (RXData); and one or more soft-input-soft-output decoders (42) coupled to the input circuit and configured to decode the data block with error correction, the one or more soft-input-soft-output decoders implemented in an integrated circuit.

Nguyen does not explicitly disclose a soft-input-soft-output decoders including, a gamma calculator; an alpha/beta recursion processor; and a log-likelihood-ratio processor coupled to the gamma calculator and the alpha/beta recursion processor and configured to provide an estimate of a transmitted data block.

However, in the same field of endeavor, Van Stralen discloses a gamma calculator (fig. 2) configured to calculate a state transition probability produced by a particular input bit of the data block; an alpha/beta recursion processor (40) configured to perform an alpha/beta recursion

process, the alpha/beta recursion processor configured to concurrently operate pipelined subprocesses that perform the alpha/beta recursion process and to store the output of each sub-process for input by a subsequent sub-process of the pipelined sub-processes; and a log-likelihood-ratio processor coupled to the gamma calculator and the alpha/beta recursion processor and configured to provide an estimate of a transmitted data block (col. 6, lines 65 through col. 7 line 35; col. 14, lines 36-61).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to combine Van Stralen's High speed turbo decoder with the High speed turbo decoder architecture, as disclosed by Nguyen. Doing so would provide a turbo decoder which efficiently uses memory and combinatorial logic such that the structure is highly streamlined with parallel signal processing.

As to claims 17-19, Nguyen discloses a sub-system, wherein the pipelined sub-processes concurrently perform a particular recursion operation of the recursion process on a plurality of samples of the data block; wherein the pipelined sub-processes concurrently perform a plurality of recursion operation of the recursion process on a particular sample of the data block; and wherein the recursion process comprises at least one of a forward recursion operation and a backward recursion operation (see [0003, 0012, 0015]).

As to claim 20, Nguyen discloses a subsystem, wherein the input circuit is configured to divide the data block into data windows; and the pipelined sub-processes are concurrently operated to perform the recursion process in decoding the data windows (fig. 6; [0012]).

As to claims 21 and 23-25, Nguyen does not explicitly disclose a sub-system, wherein the recursion process comprises an alpha/beta recursion process; and the alpha/beta recursion

process comprises an alpha recursion operation and a beta recursion operation. However, the limitation is obvious and well known in the art, as evidenced by Van Stralen's (col. 6, lines 65 through col. 7 line 35; col. 14, lines 36-61). See the motivation for the same reason disclosed in claims 16 and 30 above.

As to claim 22, Nguyen discloses a sub-system, wherein the recursion process comprises a forward/backward recursion process; and the forward/backward recursion process comprises a forward recursion operation and a backward recursion operation (figs. 13, 16).

As to claims 26-29, Nguyen (fig. 4) discloses a sub-system, wherein the pipelined sub-processes are concurrently operated to perform a plurality of recursion operations of the recursion process on a particular data window; the pipelined sub-processes concurrently perform a particular recursion operation of the recursion process on a plurality of the data windows and a plurality of recursion operations of the recursion process on a particular data window (fig. 6; [0012]). Nguyen discloses a sub-system, wherein each of the one or more processors comprise a memory element (43, 45) that stores the output of each sub-process; and wherein each of the one or more processors comprise a delay element that stores the output of each sub-process ([0007]).

As to claims 31-36, the claims have substantially the limitations of claims 16 and 30; therefore, they are analyzed as previously discussed in claims 31-32 above.

As to claims 37-38, Nguyen (fig. 4) shows a system for performing a recursion process on a data block for error correction, comprising: means for concurrently operating pipelined sub-processes of a recursion process on the data block; means for storing output data from of each sub-process; and means for inputting the output data of each sub-process to a subsequent sub-process of the pipelined sub-processes; the system further including means for dividing the encoded data block

into data windows; means for decoding the data windows with error correction using concurrently operating pipelined sub-processes of the forward/backward recursion process; and means for storing output data from each sub-process for input by a subsequent sub-process of the pipelined sub-processes (see abstract).

As to claims 1 and 5, method claims 1 and 5 correspond to apparatus claims 16 and 30 above; therefore, they are analyzed as previously discussed in claims 16 and 30 above.

As to claims 2-4, Nguyen discloses a method, wherein concurrently operating the pipelined sub-processes comprises concurrently performing a particular recursion operation of the recursion process on a plurality of samples of the data block; and wherein concurrently operating the pipelined sub-processes comprises concurrently performing a plurality of recursion operations of the recursion process on a particular sample of the data block (see [0003, 0012, 0015]).

As to claims 6-9, Nguyen discloses a method, wherein decoding the data windows comprises concurrently performing a particular recursion operation of the forward/backward recursion process on a plurality of the data windows; and wherein concurrently performing the particular recursion operation on the plurality of data windows comprises concurrently performing one of an alpha recursion and a beta recursion on the plurality of the data windows (fig. 6; [0012]).

As to claims 10-12, the claims have substantially the limitations of claims 6-9; therefore, they are analyzed as previously discussed in claims 7-9 above.

As to claims 13-15, Nguyen discloses a method, wherein concurrently operating the pipelined sub-processes comprises concurrently performing a particular recursion operation of

the forward/backward recursion process on a plurality of the data windows and a plurality of recursion operations of the forward/backward recursion process on a particular data window. Nguyen discloses a method, wherein storing the output of each sub-process comprises storing the output using a semiconductor memory (fig. 6; [0012]); and wherein storing the output of each sub-process comprises storing the output using a delay element ([0007]).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2133

December 6, 2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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